***Single Cycle Processor***

To: DR/ Gehan Naguib

Eng/ Mohamed Dakheel

***Team members:***

1-Esraa Mohsen Mohamed

2- Kerolos Girgis

3- Salma Emad Ahmed

4- Yomna Sayed Abdullah

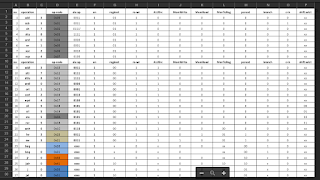
***The steps of design the processor:***

1. Pc, register file, instruction &data memories.(**kerolos girgis).**
2. **ALU (Esraa Mohsen & yomna sayed).**
3. **ALU Data Path.( Esraa Mohsen ).**
4. **Data path j-type instructions and branch ( Salma Emad).**
5. **Connections of the circuit( yomna sayed ).**
6. **Control signals table** (Salma Emad & kerolos girgis ).50/50
7. **Control unit (kerolos girgis &**  **Salma Emad )**
8. **Translating test code to machine language and entering instructions to memory( Salma Emad ).**
9. **Following the Execution of the program and evaluating the final values ( Salma Emad).**
10. **Repairing problems and errors in the design (Salma Emad)**
11. **Making the documentation and the report ( yomna sayed)**

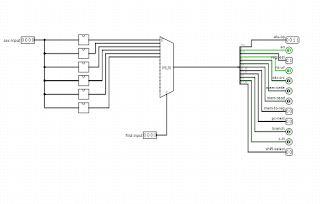
***The brief description of each component:***

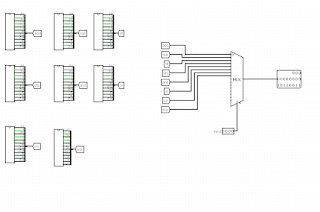
***1-Control unit:-***

As it shown in the table, each type of operations has the same most significant hexadecimal bit, like 0x0 for R-Type, or 0x1 for I-Type…. Etc So we made 6 groups of opearation which have opcodes (0x0, 0x1, 0x2, 0x3, 0x4, 0x5)

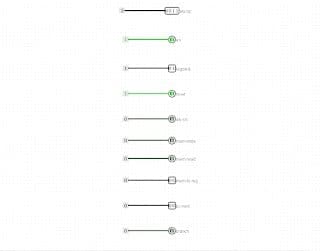


In the control unit we see that the most significant bit chooses the operation type and the least significant bit works as a selector for a multiplexer decides which instruction to do finally

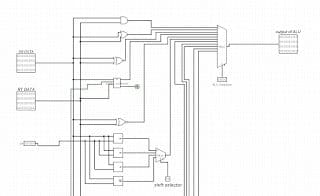


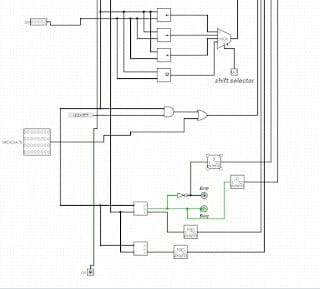
We made each type of instructions in a block, as shown previously. Each block of these has their own instructions entered as shown below, for example this is the block of R-Type instructions

And this is the block of add, for example



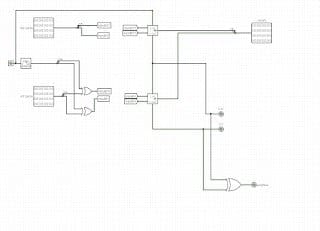
***2- ALU :***





It’s a block taking (RS data, RT data, shift amount, immediate value and constant value 0Xffff ) as inputs.

Also takes 3 signals from control unit (cin, shift selector and ALU op)

cin is to choose if it’s desirable to make addition or subtraction in the block called “ adder subtractor” 

Shift selector chooses which shift operation to do, (sll, srl, sra, ror)

ALU op is the selector of a MUX chooses what operation will the ALU does

ALU does the following operations:

Loical operations: OR, AND, XOR, XNOR

Arithmatic operation: add - subtract

Shifting operation: sll, srl, sra and ror

Operations depends on comparing 2 values (beq, bne, SLT, SLTU)

SETH by oring the shifted immediate value with the “anded RS data with constant value 0xffff ”

ALU has 2 outputs:

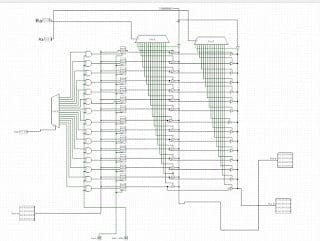
the result of “logical, arithmetic, shifting or comparing operation”

A flag for overflow

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***3-Register File***

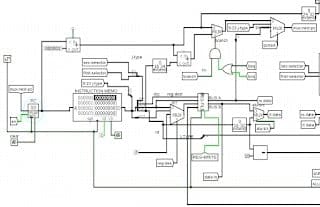
A register file is an array of processor registers in a central processing unit -(CPU). Modern integrated circuit - based register files are usually implemented by way of fast static RAMs with multiple ports.

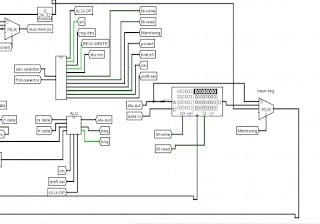


4-Data-path

A data-path is a collection of functional units, such as arithmetic logic unit or multipliers that perform data processing operations, registers and buses. Along with the control unit it composes the central processing unit (The CPU).

Simply the control unit receives external instructions or commands which it converts to into a sequence of control signals that the control unit applies to the data-path to implement a sequence of register transfer level operations





**5- PC next :-**

